Electronic Version
Stylesheet Version v1.1.1

[APPARATUS AND METHOD FOR HIGH FREQUENCY STATE MACHINE DIVIDER WITH LOW POWER CONSUMPTION]

Abstract

A digital frequency divider apparatus includes a plurality of next-state generator elements receiving an input clock signal thereto, and configured to generate a next value for each of a corresponding plurality of internal state variables. A plurality of flip-flop elements is configured to store the generated next values for the plurality of internal state variables, the plurality of flip-flop elements further configured to provide a present value of the plurality of internal state variables to the next-state generator elements through a feedback path therebetween. The generated next values for the plurality of internal state variables are based upon the present values of the plurality of internal state variables and the input clock signal.